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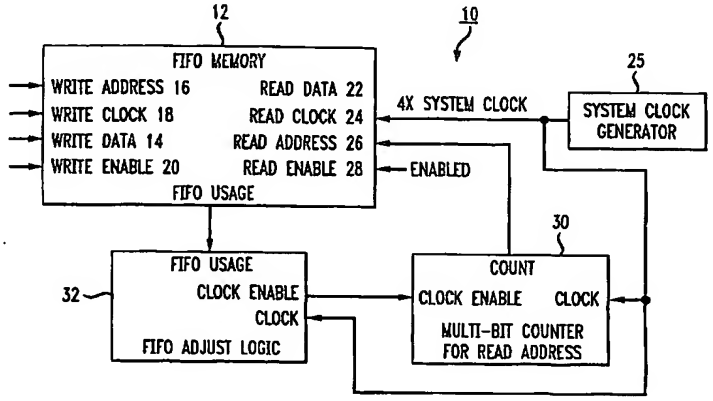
[Continued on next page]

(54) Title: ASYNCHRONOUS JITTER REDUCTION TECHNIQUE



If Fifo Usage = OK
!FifoAdjustSequnce
if Fifo Usage = Empty or Almost Empty
Start FifoAdjust Sequence & Repeat
if Fifo Usage = Full or Almost Full
Start FifoAdjustSequence & Drop
If !FifoAdjustSequence
Clock Enable every 4th clock cycle
If FifoAdjustSequence & Drop
Clock Enable after 3rd clock cycle
If FifoAdjustSequence & Repeat
Clock Enable after 5th clock cycle

Note FifoAdjustSequence drop 4 1/4samples over a period of time.

(57) Abstract: The amount of jitter incurred when reading data written into a FIFO (12) can be reduced by clocking the FIFO with Read Clock pulses at a frequency x fn where x is a whole integer and fn is the frequency at which the memory is clocked to write data. Read Addresses are applied to the FIFO at a frequency on the order of fn to identify successive locations in the memory for reading when the memory is clocked with read clocked pulses to enable reading of samples stored at such successive locations. The duration of at least one successive Read Addresses is altered in response to memory usage status to maintain memory capacity below a prescribed threshold.

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